REMARKS

Summary of the Office Action

Claims 7-12 remain in the application for reconsideration.

In the Office Action mailed August 9, 2004, the examiner rejected 7-11 under 35 U.S.C. §103(a) as being unpatentable over Nakajima in view of Osari. The examiner indicates that Nakajima teaches all steps of the invention except forming an ONO insulating layer on the entire structure. The examiner, however, cites Osari to meet the asserted deficiency of Nakajima.

The examiner only objected to claim 12 as being dependent upon a rejected base claim, but would otherwise be allowable.

Rejection Under 35 U.S.C. §103(a)

In reply, applicant believes the examiner applied Nakajima too broadly as the reference does not show all that the examiner contends. In his analysis under §103(a), the examiner incorrectly states that Nakajima shows the step of "forming an insulating film (FIG. 23(b), 80) *on the entire structure* and forming a second polysilicon film (FIG. 23(b): 71) on the insulating film 80." A closer examination of Nakajima's disclosure fails to show this step. At col. 4, line 11, Nakajima provides an insulating film 80 formed on polysilicon 70. There, Nakajima FIG. 23(B) shows forming insulating film 80 on polysilicon layer 70 only, but not the entire structure, as claimed. The resulting structure in Nakajima also differs because the level of insulating layer 80 in the cell region differs from the level of the insulating layer 74 in the peripheral circuit region. As explained below, layers 80 and 74 are formed in different steps.

In addition, the examiner incorrectly contends that Nakajima discloses the step of "patterning the second polysilicon film 71 on the insulating film 80 so that they can remain only in a given region of the cell region and the peripheral circuit region, thus forming a control gate (FIG. 23(c), 7) on the insulating film (FIG. 23(c), 15) covering the floating gate 14 in the cell region and a gate (FIG. 23(c), 4) on the insulating film (FIG. 23(c). 13) covering the surface of the substrate (FIG. 23(a), 20) in the peripheral circuit

region." Contrary, the alleged insulating film in Nakajima (as construed by the examiner) is formed in two steps – not one step as provided by claim 7. In Nakajima, see insulating film 74 of Fig. 23(a) and insulating film 80 of Fig. 23(b). These are not formed in the same layer. Thus, the examiner incorrectly equates the single-layer step of claim 7 with Nakajima's two-layer step of providing insulating film 80 (Fig. 23(B)) and insulating film 74 (Fig. 23(B)).

Accordingly, Nakajima fails as a primary reference under §103(a) because it does not disclose at least two elements or steps recited in claim 7. See, MPEP § 2143.03 (all elements must be shown in the prior art to make out a prima facie case of obviousness).

Osari, on the other hand, is cited for its showing of providing an ONO structure as an insulating layer. Applicant also notes the examiner's assertion that Osari discloses providing an ONO insulating layer *on the entire structure,* but this also differs from the ONO layer of claim 7, which lies in both the memory cell region and the peripheral circuit region. Thus, Osari is deficient because it too fails to show "patterning said second polysilicon film and said insulating film so that they remain in a given region of said cell region and said peripheral circuit region, thus forming a control gate on the insulating film covering the floating gate in said cell region, and a gate on the insulating film covering a surface of the substrate in said peripheral circuit region" (underlining added).

Accordingly, the combined teachings of Nakajima and Osari fail to suggest applicant's invention under 35 U.S.C. §103(a).

Moreover, claim 12 apparently was allowed because the cited references do not teach or suggest the claimed ONONO layer as an insulating layer. Using this same analogy, claim 11 should also be allowable by virtue of claiming an ONON layer as an insulating layer, which also is not shown or suggested by the applied art.

Last, the examiner should note that applicant made amendments to claim 7 to clarify the patentable distinction of forming an ONO insulating layer over the entire structure, and that gates formed thereby lie both in the memory cell region and the peripheral circuit region. Further, certain words, i.e., "can only," "only," and "can" were deleted as being

unnecessary limitations.

Conclusion

In view of the foregoing, applicant requests favorable reconsideration.

A petition for an automatic one-month extension of time and petition fee accompanies this paper.

Respectfully submitted,

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